Electronic Version
Stylesheet Version v1.1.1

AUTO-LINKING OF FUNCTION LOGIC STATE WITH TESTCASE REGRESSION LIST

Abstract

A method and system for identifying logic function areas, which make up a virtual machine, that are affected by specific testcases. A Hardware Descriptor Language (HDL) is used to create a software model of the virtual machine. A simulator compiles and analyzes the HDL model, and creates a matrix scoreboard identifying logic function areas in the virtual machine. A complete list of testcases is run on the virtual machine while a monitor correlates each testcase with affected logic function areas to fill in the matrix scoreboard. When a subsequent test failure occurs, either because of a modification to a logic function area, or the execution of a new test, all logic function areas that are affected, either directly or indirectly, are identified.